## SCHOTTKY BARRIER QUANTUM WELL RESONANT TUNNELING TRANSISTOR

## TECHNICAL FIELD

[0001] This application relates to a semiconductor device, specifically, a semiconductor transistor device suitable for analog and digital circuits.

## BACKGROUND OF THE INVENTION

[0002] In the past four decades, the integrated circuit industry has followed a dramatic path of shrinking device dimensions and increasing chip sizes, resulting in steady increases of performance and functionality. New generations of devices have appeared in every two to three years, following the so-called "Moore's Law". Each new generation has approximately reduced transistor size by 30%, increased circuit performance by about 40%, doubled logic circuit density, and quadrupled memory capacity comparing to the previous generation. The consistency of this advancement has led to an expectation that faster and more powerful chips will continue to be introduced on the same schedule in the foreseeable future.

[0003] The metal oxide semiconductor field effect transistor (MOSFET) constitutes the fundamental building block of semiconductor technology. A large part of its success is due to the fact that it can be continuously scaled down to smaller dimensions while increasing circuit performance and lowering manufacturing cost. The ability to consistently improve performance while decreasing power consumption has made CMOS architecture the dominant technology for integrated circuits. The scaling of CMOS transistors has been the primary factor driving the improvement in microprocessor performance. In order to maintain such rapid rate of improvement, aggressive scaling of MOS devices presents considerable challenges to the semiconductor industry. The industry generally expects that within a decade or so, MOS-FET will encounter critical technological barriers and fundamental physical limitations to size reduction. The major challenges include power consumption control, leakage current reduction, driving current improvement, thin gate insulators with high dielectric constant, metal gates with appropriate work functions, ultra-shallow source/drain junctions, parasitic resistance/capacitance reduction, statistical dopant fluctuation, and uniformity of device characteristics.

[0004] The most pressing limit to further miniaturization is the increase of power consumption. The power density at the chip surface is doubled for every 3.3 years. The rapid increase of heat generation is caused by insufficient reduction of power supply voltage and aggressive increase of transistor density. If the current trends in the clock frequency and the number of on-chip transistors continue, the power consumption of a high-performance microprocessor would reach 10 kW within several years and the heat generation at the chip surface would reach 1000 W/cm<sup>2</sup>. By comparison, the power density is about 100 W/cm<sup>2</sup> for a light bulb filament, 1000 W/cm<sup>2</sup> for a rocket nozzle, and 6000 W/cm<sup>2</sup> for the surface of the sun. Furthermore, it is recognized that heat can only be removed from a surface at some finite rate. The maximum rate of thermal energy that can be removed from silicon surface at T<sub>max</sub><400° K. is about 1000 W/cm<sup>2</sup> by convective cooling.

[0005] As the scaling of conventional planar bulk silicon CMOS transistors approaches its fundamental limits, innovative device structures and new materials must be considered

to continue the historic progress in transistors. Some variations of MOSFET structures are being actively studied, which include ultra-thin body (UTB) silicon-on-insulator (SOI) MOSFETs, multi-gate MOSFETs (such as FinFET and Tri-Gate), SB-MOSFETs with Schottky barrier source/drain, carbon nanotube transistors (CNTs), and graphene nano-ribbon transistors. These non-classical MOSFETs are designed to improve short-channel effects and have better scalability than the planar bulk MOSFET. However, these non-classical devices are still MOSFETs; they face similar challenges for the planar bulk MOSFETs, such as increasing power consumption and performance saturation. The current trends of increasing chip speed and functional density are difficult to maintain by the MOSFET. Silicon technology has reached a point, at which significant innovations are required to circumvent the challenges associated with continued device scaling. There is a need for a new transistor device to continue the trends of increasing circuit performance, enhancing chip functionality, and lowering manufacturing cost.

[0006] Alternative device structures other than the MOS-FET are being considered that might allow the continuation of scaling trends when physical limits of conventional MOS-FETs are eventually reached. Two prior-art devices, metal base transistors (MBT) and resonant tunneling devices, both operating on the principle of quantum mechanical tunneling, are to be discussed.

[0007] The metal base transistor was an early attempt to achieve better performance than bipolar transistors. The device structure of the MBT has three different versions, but all of them have metal for the base. The first version is a metal-insulator-metal-insulator-metal (MIMIM) structure. FIG. 1a shows the MIMIM structure and its band diagram. When the device is properly biased, electrons are injected from the emitter to the base by tunneling through a thin insulating barrier. The injected electrons are called hot electrons since they have energies more than a few kT above the Fermi level in the base. The MIMIM device is also one of the hot-electron transistors and ballistic injection transistors. The hot electrons continue to travel through the base to the collector if they are not recombined in the base. The second version of the MBT has the base-to-collector MIM structure replaced by a metal-semiconductor Schottky junction. FIG. 1b shows the metal-insulator-metal-semiconductor (MIMS) structure and its band diagram. The third version of the MBT has both MIM structures replaced by metal-semiconductor Schottky junctions. FIG. 1c shows the semiconductor-metalsemiconductor (SMS) structure and its band diagram. The SMS MBT employs thermionic emission rather than tunneling injection of hot carriers into the base because the Schottky junction has smaller emitter-to-base barrier height than the MIM structure. Early MBTs have been plagued by two major problems, which are the poor base transport factor  $\alpha_T$  due to their relatively large base widths and the difficulty of growth of good-quality single-crystal semiconductor materials on metals. Because of these problems, there has been very little development on the MBT in recent years.

[0008] A resonant tunnel device uses quantum effects to produce negative differential resistance. The device has a double-barrier quantum-well structure typically formed by the heterojunctions of III-V compound semiconductors (such as GaAs and AlGaAs) with large discontinuities in the conduction band. The electron energy in a quantum well is quantized. FIG. 2a shows the energy band diagram of a two-terminal double-barrier AlGaAs/GaAs/AlGaAs resonant